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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/777,971	02/13/2004	Naokazu Kuzuno	248965US2S	7450

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EXAMINER	
BAUER, SCOTT ALLEN	
ART UNIT	**PAPER NUMBER**
2836	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	01/05/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/777,971	KUZUNO ET AL.	
	Examiner	Art Unit	
	Scott Bauer	2836	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *03 October 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *13 February 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

1. Claims 1, 2 & 7-15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kim et al. (US 6,150,868) in view of Kim et al. (US 5,929,691) and Verwegen (US 6,147,546).

With regard to Claim 1, Kim '868, in figure 1 teaches a fuse latch circuit comprising: a fuse (70); a first inverter (INV1) in which an input end is connected to one end of the fuse; a second inverter (INV 2) in which an input end is connected to an output end of the first inverter; a first transistor (P1) in which a first power supply potential (HVCC) is input to a source, a drain is connected to the one end of the fuse, and a pulse signal (prechb) for initialization is input to a gate; a second transistor (P4) in which the first power supply potential (HVCC) is input to a source, a drain is connected to the one end of the fuse, and a gate is connected to the output end of the first inverter; and a third transistor (N1) in which a second power supply potential (GND) is input to a

source, a drain is connected to the other end of the fuse, and a pulse signal (ADDR) is input to a gate.

Kim '868 does not teach that gate of the first transistor (P1) has the same pulse signal input to the gate of the third transistor (N1) and that the conductance of the first transistor is higher than that of the second transistor wherein the pulse is used to program a fuse (31).

Kim '691, in Figure 7, teaches an anti-fuse programming circuit wherein the gates of a first and third transistor are coupled to the same pulse signal (ØC).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of Kim et al. '868 with Kim et al. '691 by using the same pulse (ØC) as taught by Kim '691 to drive the gates of the first and third transistors (P1 & N1) as taught by Kim '868 for the purpose of constructing a less complex circuit requiring fewer bus lines and thus making room for more anti-fuse circuits on a chip.

In the Kim '868 reference, it is not imperative that the pre-charge signal goes high before the address signal goes high, as the anti-fuse would still be programmed if the two signals were received at the same time.

Verwegen teaches a zero volt/current fuse arrangement wherein a fuse (2) is coupled to the drains of a PFET (6) and NFET (7) transistor. The source of the PFET is coupled to a first power supply terminal (Vdd) and the source of the NFET is connected to a second power supply terminal. Verwegen further states that the PFET (6) has a large W/L ratio and that the NFET (7) has a small W/L ratio (column 3 lines 41-56).

Thus causing the conductance of the first transistor to be higher then the conductance of the second transistor as the conductance is proportional to the transistor's W/L ratio.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of Kim et al. in view of Kim et al. (US 6150868) with Verwegen, by selecting the sizes of the first and second transistors so that the first transistor has a higher conductance than that of the second transistor as taught by Verwegen, for the purpose of insuring that the voltage at the input of the inverter (35) is stable enough to be read as a logical "1" or a logical "0" (Verwegen column 3 lines 52-56).

With regard to Claim 2, Kim et al. '868 in view of Kim et al. '691 and Verwegen discloses the fuse latch circuit of Claim 1. Kim et al. '868 further discloses that a circuit threshold value of the first inverter (INV1) is set to a half value of a total value of the first power supply potential and the second power supply potential (HVCC).

With regard to Claim 7, Kim et al. '868 in view of Kim et al. '691 and Verwegen, discloses the fuse latch circuit of Claim 1. Kim et al. '868 further discloses that the third transistor (20) is formed immediately below the end portion of the fuse (70).

With regard to Claim 8, Kim et al. '868 in view of Kim et al. '691 and Verwegen, discloses the fuse latch circuit of Claim 1. Kim et al. '868 further discloses that the fuse latch circuit is used for a redundancy circuit of memory (column 1 lines 16-18).

With regard to Claim 9, Kim et al. '868 in view of Kim et al. '691 and Verwegen, discloses the fuse latch of Claim 1.

Verwegen further discloses that the fuse can be an aluminum fuse (column 1 lines 44-49).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of Kim et al. '868 with Verwegen, since it has been held to be within the general skill of a worker in the art to select a known material on the basis of its suitability for the intended use as a matter of obvious design choice. *In re Leshin, 125 USPQ 416.*

With regard to Claim 10, Kim et al. '868 in view of Kim et al. '691 and Verwegen, discloses the fuse latch of Claim 1.

Kim et al. '691 further discloses that the fuse can be an electrical fuse (column 1 lines 29-32).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of Kim et al. '868 with Kim '691, since it has been held to be within the general skill of a worker in the art to select a known material on the basis of its suitability for the intended use as a matter of obvious design choice. *In re Leshin, 125 USPQ 416.*

With regard to Claim 11, Kim et al. '868 in view of Kim et al. '691 and Verwegen, discloses the fuse latch of Claim 1. Kim et al '868 in Figure 1, further discloses that the first transistor and second transistor are each a p-channel MOS transistor.

With regard to Claim 12, Kim et al. '868 in view of Kim et al. '691 and Verwegen, discloses the fuse latch of Claim 1. Kim et al. '868, in Figure 1, further discloses that the third transistor is an n-channel MOS transistor.

With regard to Claim 13, Kim et al. '868 in view of Kim et al. '691 and Verwegen, discloses the fuse latch of Claim 1. Kim '868, in Figure 1, further discloses that the second power supply potential is a ground potential.

With regard to Claim 14, Kim et al. '868 in view of Kim et al. '691 and Verwegen, discloses the fuse latch of Claim 1. Kim '868 further discloses that the output signal (repb) of the second inverter is fed into an internal circuit (column 3 lines 16-23).

With regard to Claim 15 Kim et al. '868 in view of Kim et al. '691 and Verwegen discloses the fuse latch of Claim 1. Kim et al. '868, further discloses that fuse latch circuit is part of a memory (column 1 lines 16-18).

2. Claims 3 & 16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kim et al. '868 in view of Kim et al. '691 and Verwegen, and further in view of Saito et al. (US 6,320,800).

With regard to Claim 3, Kim et al. '868 in view of Kim et al. '691 and Verwegen, discloses the fuse latch circuit according to Claim 1 wherein the fuse latch circuit is part of a semiconductor memory device (Kim '868 column 1 lines 16-18) which is a semiconductor integrated circuit.

Kim et al. '868 in view of Kim et al. '691 and Verwegen, does not teach that a plurality of the fuse latch circuits of Claim 1 form a fuse latch circuit group and that an internal circuit receives output signals of the fuse latch group.

Saito et al., in Figure 1, teaches a semiconductor memory having redundant circuitry comprising: a fuse circuit group (201) comprised of a plurality fuse circuits; and an internal circuit (101) which receives output signals of the fuse latch circuit group.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of Kim et al. '868 in view of Kim et al. '691 and Verwegen, with Saito et al., by placing the fuse latch circuit taught by Kim et al. '868 in view of Kim et al. '691 and Verwegen, in the redundant column cell array fuse circuit (201) taught by Saito et al., for the purpose of using the fuse latch of Kim et al. '868 in view of Kim et al. '691 and Verwegen, to replace a defective cell in a memory cell array, thereby providing a faster method of memory read/write operations for an entire array of memory.

Further, Kim et al. '868 in view of Kim et al. '691 and Verwegen, discloses the claimed invention of Claim 3 except that the fuse latch of Claim 1 is not arranged into a fuse latch group. It would have been obvious to one having ordinary skill in the art at the time the invention was made to arrange the fuse latch taught by Kim et al. '868 in view of Kim et al. '691 and Verwegen, into a group of many fuse latch circuits, since it has been held that mere duplication of the essential working parts of a device involves only routine skill in the art. St. Regis Paper Co. v. Bemis Co., 193 USPQ 8.

With regard to Claim 16 Kim et al. '868 in view of Kim et al. '691, Verwegen and Saito discloses the fuse latch of Claim 3. Kim et al. '868, further discloses that fuse latch circuit is part of a memory (column 1 lines 16-18).

3. Claims 4 - 6 & 17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kim et al. '868 in view of Kim et al. '691, and Verwegen, and further in view of Saito et al. and Kang (US 6,134,177).

With regard to Claim 4, Kim et al. '868 in view of Kim et al. '691 and Verwegen, teaches the fuse latch circuit according to Claim 1 wherein the fuse latch circuit is part of a semiconductor memory device (Kim '868 column 1 lines 16-18) which is a semiconductor integrated circuit.

Kim et al. '868 in view of Kim et al. '691 and Verwegen, does not teach a plurality of fuse latch circuit groups each comprised of a plurality of the fuse latch circuits; an

internal circuit which receives output signals of said plurality of fuse latch circuit groups, and that the pulse signals are individually fed with different timings into said plurality of fuse latch circuit groups.

Saito et al., in Figure 1, teaches a semiconductor memory having redundant circuitry comprising: a plurality of fuse circuit groups (201a-c) comprised of a plurality fuse circuits; and an internal circuit (101) which receives output signals of the fuse latch circuit group.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of Kim et al. '868 in view of Kim et al. '691 and Verwegen, with Saito et al., by placing the fuse latch circuit taught by Kim et al. '868 in view of Kim et al. '691 and Verwegen, in the redundant column cell array fuse circuit (201) taught by Saito et al., for the purpose of using the fuse latch of Kim et al. '868 in view of Kim et al. '691 and Verwegen, to replace a defective cell in a memory cell array, thereby providing a faster method of memory read/write operations for an entire array of memory.

Further, Kim et al. '868 in view of Kim et al. '691 and Verwegen, discloses the claimed invention of Claim 3 except that the fuse latch of Claim 1 is not arranged into a fuse latch group within a plurality of fuse latch groups. It would have been obvious to one having ordinary skill in the art at the time the invention was made to arrange the fuse latch taught by Kim et al. '868 in view of Kim et al. '691 and Verwegen, into a group of many fuse latch circuits, since it has been held that mere duplication of the essential

working parts of a device involves only routine skill in the art. St. Regis Paper Co. v. Bemis Co., 193 USPQ 8.

Kang, in Figure 4, teaches a redundancy decoding circuit wherein the pulses to the fuse latch circuits (10) are individually fed with different timings into a plurality of fuse latch circuit groups (column 4 lines 13-25).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings Kim et al. '868 in view of Kim et al. '691 and Verwegen, with Kang, by driving the fuse latch circuit groups taught by Kim et al. '868 in view of Kim et al. '691 and Verwegen, with the pulse generator (20) taught by Kang, by driving each fuse latch circuit group with a different flip-flop output (Q0-Q3) for the purpose of reducing standby current during read/write operations (Kang column 4 lines 9-12).

With regard to Claims 5 & 6, Kim et al. '868 in view of Kim et al. '691, Verwegen, Saito et al. and Kang discloses the semiconductor integrated circuit according to Claim 4. Kang, in Fig. 5, further teaches that the pulse signals (Q0-Q3) to be individually input to said plurality of fuse latch circuit groups, do not overlap timewise with one another (normal read/write mode). Kang further teaches that the timings with which the pulse signals according to claim 1 are individually fed into said plurality of fuse latch circuit groups are controlled by a delay circuit (20) having a delay time longer than at least a width of the pulse signal, as demonstrated in Figure 5.

With regard to Claim 17 Kim et al. '868 in view of Kim et al. '691 and Verwegen, Saito et al. and Kang discloses the fuse latch of Claim 4. Kim et al. '868, further discloses that fuse latch circuit is part of a memory (column 1 lines 16-18).

4. Claim 18 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kim et al. '868 in view of Kim et al. '691 and Verwegen, and further in view of Potter et al. (US 6,308,230).

With regard to Claim 18, Kim et al. '868 in view of Kim et al. '691 and Verwegen teaches the fuse latch element of Claim 1 wherein the fuse latch is part of a semiconductor integrated circuit memory.

Kim et al. '868 in view of Kim et al. '691 and Verwegen, does not teach that the memory is in a memory embedded microcomputer.

Potter et al., teaches that a memory array can be embedded in a microcomputer.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of Kim et al. '868 in view of Kim et al. '691 and Verwegen, and Saito et al. with Potter et al., by placing the memory taught Kim et al. '868 in view of Kim et al. '691 and Verwegen, and Saito et al., in the memory embedded microcomputer taught by Potter et al., for the purpose of saving cost and space on a circuit board by integrating two separate semiconductor integrated circuits into one integrated circuit.

5. Claim 19 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kim et al. '868 in view of Kim et al. '691, Verwegen and Saito et al., and further in view of Potter et al. (US 6,308,230).

With regard to Claim 19, Kim et al. '868 in view of Kim et al. '691 and Verwegen, and Saito et al. teaches the fuse latch element of Claim 3 wherein the fuse latch is part of a semiconductor integrated circuit memory.

Kim et al. '868 in view of Kim et al. '691, Verwegen, and Saito et al. does not teach that the memory is in a memory embedded microcomputer.

Potter et al., teaches that a memory array can be embedded in a microcomputer.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of Kim et al. '868 in view of Kim et al. '691 and Verwegen, and Saito et al. with Potter et al., by placing the memory taught Kim et al. '868 in view of Kim et al. '691 and Verwegen, and Saito et al., in the memory embedded microcomputer taught by Potter et al., for the purpose of saving cost and space on a circuit board by integrating two separate semiconductor integrated circuits into one integrated circuit.

6. Claim 20 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kim et al. '868 in view of Kim et al. '691 and Verwegen, Saito et al., Kang, and further in view of Potter et al. (US 6,308,230).

With regard to Claim 20, Kim et al. '868 in view of Kim et al. '691, Verwegen, Saito et al. and Kang teaches the fuse latch element of Claim 4 wherein the fuse latch is part of a semiconductor integrated circuit memory.

Kim et al. '868 in view of Kim et al. '691 and Verwegen, and Saito et al. and Kang does not teach that the memory is in a memory embedded microcomputer.

Potter et al., teaches that a memory array can be embedded in a microcomputer.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of Kim et al. '868 in view of Kim et al. '691, Verwegen, Saito et al. and Kang with Potter et al., by placing the memory taught Kim et al. '868 in view of Kim et al. '691, Verwegen, Saito et al. and Kang, in the memory embedded microcomputer taught by Potter et al., for the purpose of saving cost and space on a circuit board by integrating two separate semiconductor integrated circuits into one integrated circuit.

Response to Arguments

Applicant's arguments filed 03 OCT 06 have been fully considered but they are not persuasive. With regard to Applicants' arguments starting on page 7, Applicants state that Kim '868 does not teach a fuse which uses a laser, however, claim 1 recites "a fuse". As such, the antifuse of Kim '868 can be broadly defined as a fuse and thus teaches the claim language. Applicants further argue that Kim '868 has six disadvantages over the claimed invention. However, these disadvantages do not prevent Kim '868 from disclosing the recitations of claim 1. On Page 8 Applicants argue

that the Kim '691 patent teaches that a fuse is places between FET 34 and ground instead of between the two FET's that form an inverter. Applicants then argue that none of the previously cited references teach the structure of the claimed invention. However, one cannot show nonobviousness by attacking references individually where the rejections are based on combinations of references. See *In re Keller*, 642 F.2d 413, 208 USPQ 871 (CCPA 1981); *In re Merck & Co.*, 800 F.2d 1091, 231 USPQ 375 (Fed. Cir. 1986). Kim '868 teaches the structure of the claim except that the same pulse signal is input into the gate of the first and third inverters. The Kim '961 is combined with the Kim '868 reference to teach that the two transistors can be driven as an inverter to program the fuse.

Applicants further argue that the two references contain conflicting teaches in that the fuse of Kim '868 is not directly connected to a power source (ground) while the fuse of Kim '961 is connected directly to ground. The Kim '961 reference was used to teach a programmable fuse environment wherein two transistors are driven by a single pulse signal. Kim '961 is not relied on to teach the placement of the fuse in the circuit. Kim '868 is relied on to teach the placement of the fuse in the circuit. The fact that the fuses are placed on different sides of the NFET does not mean that the two references are not combinable, as both fuses do not conduct current when the pulse signal is not applied, and conduct current when the signal is applied.

Lastly, Applicants argue that the rejection of claim 2 is improper. However, Kim '868 teaches that the inverters (INV1 & 2) are supplied with HVCC, which is half the voltage of VCC (Kim '868 column 3 lines 20-23).

Conclusion

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Scott Bauer whose telephone number is 571-272-5986. The examiner can normally be reached on M-F 8am-5pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Brian Sircus can be reached on 571-272-2058. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

SAB

26 DEC 06

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